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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/975,104	10/10/2001	Warren Snyder	CYPR-CD00183	8786

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EXAMINER	
BRODA, SAMUEL	
ART UNIT	**PAPER NUMBER**
2123	

DATE MAILED: 03/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/975,104	SNYDER, WARREN	
	Examiner	Art Unit	
	Samuel Broda	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 October 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/15/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-17 have been examined.

Priority

2. This Application contains a claim for the benefit of priority to U.S. Provisional Application No. 60/243,708 filed 26 October 2000. The provisional application has been reviewed and priority is denied, because the provisional application does not appear to enable the claimed invention as required under 35 U.S.C. Section 112, first paragraph. See 35 U.S.C. 119(e)(1).

For example, the provisional application contains a set of 'powerpoint-style' drawings and datasheets describing desired features for a microcontroller or a 'system-on-chip,' but this material does not appear to contain either the text description or the drawings found in the Application.

Drawings

3. Applicant's formal drawings have been reviewed and approved.

Claim Rejections - 35 U.S.C. § 112, Second Paragraph

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4.1 Claims 1-17 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the elements. See MPEP § 2172.01. The omitted elements are the design of the DUT (or microcontroller device) containing one data interface line and one clock line.

Although are claims are written in method format, features of the structural design of DUT are necessary to accomplish the claimed methods. The essential feature of the DUT is described in the Specification at page 21 lines 19-24, stating the following:

> The present invention provides for full in-circuit emulation without need for a special bond-out version of a DUT. This is accomplished using a minimal amount of design embedded within the DUT itself. In the current embodiment, the only functionality required of the production microcontroller itself is to provide for transfer of data over one or two lines forming the data portion of the interface and at least one clock (the data clock, the microcontroller clock is optional).

Claim Rejections - 35 U.S.C. § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> . . .
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5.1 Claims 1-2 and 8-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Beck et al, U.S. Patent 5,493,723, issued 20 February 1996.

5.2 Regarding claims 1 and 8, Beck et al teaches a method of obtaining debug information, comprising:

executing a sequence of instructions by a device under test (DUT) [master CPU 10];

executing the sequence of instructions by an emulator device emulating the functions of the DUT and executing the sequence of instructions in lock-step fashion with the DUT [microprocessor ISE CPU 12 operating as in-system emulator, column 2 line 55 through column 3 line 29];

the DUT conveying I/O read information to the emulator device [master CPU 10 and ISE CPU 12 connected by lines 18 and 19, Fig. 1]; and

a host computer system reading real-time state and debug information from the emulator device without interrupting the DUT [ISE system 24 reading state and debug information from ISE CPU 12 via lines 19 and 26 without interrupting master CPU 10].

Therefore, Beck et al anticipates claims 1 and 8.

5.3 Regarding claim 9, this claim is anticipated by Beck et al using the reasoning of claim 1 in which both master CPU 10 and ISE 12 inherently contain microcontroller devices.

5.4 Regarding claims 2 and 10, the processor emulation system of Beck et al operates in a cycle with a data transfer phase (prior to and after reset) and a control phase (reset). See column 4 line 49 through column 5 line 26.

Allowable Subject Matter

6. Claims 3-7 and 11-17 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to Applicant's disclosure. Reference to Veenstra et al, U. S. Patent 6,704,889 issued 9 March 2004 (having priority to 6 November 1998) is cited as teaching embedding a logic analyzer in a programmable logic device.

Reference to Miyamori et al, U. S. Patent 5,978,937 is cited as teaching a microprocessor having a processor core connected to a debug module via an internal debug interface, and having an external debug interface.

Reference to Coker, U. S. Patent 5,371,878 is cited as teaching a target embedded computer system connected to a shadow system via an interface.

Reference to Marsh, "Smart Tools Illuminate Deeply Embedded Systems," EDN, Vol. 45 No. 3, pp. 129-138 (3 February 2000), is cited as teaching a review of instruction-set simulators applied to real-time operating systems.

Reference to Huang et al, "ICEBERG: An Embedded In-circuit Emulator Synthesizer for Microcontrollers," Proceedings of the 36th Design Automation Conference, pp. 580-585 (June 1999), is cited as teaching a tool to insert and integrate in-circuit emulation circuitry into an RTL core of a microcontroller.

Reference to York et al, "On-chip Support Needed for SOC Debug," Electronic Engineering Times, pp. 104, 110 (14 June 1999), is cited as teaching the embedding of a real-time trace subsystem within a system-on-chip incorporating an embedded trace macrocell, a trace port analyzer, and trace debug tools.

8. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Samuel Broda, whose telephone number is (571) 272-3709. The Examiner can normally be reached on Mondays through Fridays from 8:00 AM – 4:30 PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Kevin Teska, can be reached at (571) 272-3716. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the group receptionist, whose telephone number is (571) 272-2100.

SAMUEL BRODA, ESQ.
PRIMARY EXAMINER